IN THE SPECIFICATION:

Page 1

Between the Title and the heading "BACKGROUND OF THE INVENTION," please insert the following heading and paragraph:

"CROSS-REFERENCE TO RELATED APPLICATIONS"

This application is a Continuation application of Application Serial No. 09/880,819, filed June 15, 2001, the entire disclosure of which is hereby incorporated by reference.

Page 5

Please replace paragraph [0013] with the following new amended paragraph:

Fig. 16 is an essential part circuit diagram for explaining ~~other~~another example of a memory circuit of a ~~stick~~static memory type described in Fig. 2(b) of Japanese Laid-open Patent Publication 194205/1996. In the drawings, a portion surrounded by a chained line indicates a pixel memory. This circuit is comprised of switching elements 21, 22, 23 and 24 which are formed of thin film transistors arranged at intersecting portions between scanning lines 3 and signal lines 4. The switching elements 22, 23 constitute an inverter and forms a memory circuit. A scanning voltage (pulse) is applied to the scanning line 3 and, in synchronism with this step, a signal which controls the opening/closing of the switching element 24 is inputted to the switching element 21 though the signal line 4.

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Please replace paragraph [0030] with the following new amended paragraph:

On a still another side of the pixel memory array, an applying pad ~~VCON-P~~ VCOM-P of the fixed voltage VCOM is mounted.

Please replace paragraph [0031] with the following new amended paragraph

Then, on the side on which the applying pad ~~VCON-P~~ VCOM-P of the fixed voltage VCOM is mounted, applying pads PBP-P and PBN-P for two kinds of voltages PBP and PBN which differ every field are mounted and alternating voltage lines PBP-L and PBN-L which are connected to these applying pads PBP-P and PBN-P are extended toward the pixel PIX.